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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,718	02/27/2004	Lawrence A. Booth	P8451C	6787

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INTEL CORPORATION
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EXAMINER	
NAMAZI, MEHDI	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,718	BOOTH, LAWRENCE A.	
	Examiner	Art Unit	
	Mehdi Namazi	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,7,9,10 and 18-23* is/are rejected.

7)☒ Claim(s) *4,5,8 and 11-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to application filed February 27, 2004.

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.

(b) CROSS-REFERENCE TO RELATED APPLICATIONS.

(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.

(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT

(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or

REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)

(f) BACKGROUND OF THE INVENTION.

1. Field of the Invention.

2. Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.

(g) BRIEF SUMMARY OF THE INVENTION.

(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).

(i) DETAILED DESCRIPTION OF THE INVENTION.

(j) CLAIM OR CLAIMS (commencing on a separate sheet).

(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).

(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Specification

The disclosure is objected to because of the following informalities: The brief summary of the invention is missing.

Appropriate correction is required.

Drawings

The drawings are objected to because figures 3, and 4, elements 300, and 410 respectively "line buffer" should be replaced with --loop buffer-- (see specification page 9). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the

unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321 may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-23 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-15 of U.S. Patent No. 6,757,817.

A question of patentability is raised with respect to representative claims 1 and 4 of the instant application under the judicially doctrine of "obviousness-type" double patenting with respect to U.S. Patent No. 6,757,817.

More specifically, OPQR maintains that in view of the "obviousness-type" double patenting rationale enunciated in Georgia pacific Corp v United States Gypsum Co., 52 USPQ2d 1590, U.S. Court of Appeals Federal Circuit 1999, representative claims 1 and

4 merely define an obvious variation of the invention claimed in US Patent number 6,757,817.

Initially it should be noted that the present application is related to Patent No. 6,757,817 having the same inventive entity. The Assignee for both applications is Intel Corporation. The entire disclosures of the both application and Patent are identical.

Claim 1, of the Patent Number 6,757,817 is compared to claims 1 and 4 of instant application in the table below.

Limitations in Pending Application (10/788,718)	Limitations in Patent No. 6,757,817
1. **A method of executing an instruction comprising: determining if at least a portion of the instruction is stored in a loop buffer; and determining if at least a portion of the instruction is stored in a cache.**	1. **A method of executing an instruction comprising: determining if at least a portion of the instruction is stored in a loop buffer; and determining if at least a portion of the instruction is stored in a cache,**
4. the method of claim 1, Wherein determining if at least a portion of the instruction is in a loop buffer includes determining if at least a portion of the instruction is in first portion of a memory array, and wherein determining	**wherein determining if at least a portion of the instruction is in a loop buffer includes determining if at least a portion of the instruction is in first portion of a memory array, and wherein determining if at least a portion of the**

if at least a portion of the instruction is in the cache includes determining if at least a portion of the instruction is in a second portion of the memory array.	**instruction is in the cache includes determining if at least a portion of the instruction is in a second portion of the memory array.**

Claims 1-23 of the instant application are anticipated by the Patent claims 1-15 of 6,757,817, in that claims 1-15 of that Patent 6,757,817 contain all the limitations of claims 1-23 of the instant application. Claims 1-23 of the instant application therefore are not patently distinct from the earlier patent claims and as such are unpatentable for obvious-type double patenting.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al. (5,353,426) in view of Fleck et al. (6,085,315).

With regard to claim 1, Patel teaches method of executing an instruction comprising:

a) determining if an instruction information portion (see the information relating to the

instruction in col.8, lines 48-68, co1.9, lines 1-2) is stored in a buffer (see fig.5 [88], col.9, lines 18-24, see also co1.8, lines 48-68, col.9, lines 1-2 for the instruction information stored in the buffer); and

b) determining if a portion of an instruction is stored in a cache (see fig.5 [84], see the cache hit in co1.9, lines 10-12, see the subset of instruction stored in cache 44 in col.3, lines 10-13, col.5, lines 47-56, see how the cache tag 46 related to the cache 44 in col.3, lines 18-24, col.7, lines 67-68, co1.8, lines 1-4, see also col.8, lines 31-41 for the tag matching operation).

Patel did not specifically teach his buffer was a loop buffer as claimed. However, Fleck disclosed a cache system for including a loop buffer [loop cache buffer] for storing and providing information of instructions executed in a loop (e.g see co1.3, lines 25-67, col.4, lines 1-17). It would have been obvious to one of ordinary skill in the art to use Fleck in Patel for using the loop buffer for determining if at least a portion of the instruction was stored in a buffer as claimed because the use of Fleck's loop buffer could provide the capability to reduce the number of times of a given request made frequently to the Cache array of Patel, thereby minimizing the R/W cycle, and it could be achieved by defining the I/O ports of the loop buffer of Fleck into Patel's configuration, and because Patel already taught the use of a buffer [cache miss buffer] in addition to a cache to reduce the wait time (e.g see col.3, lines 48-53), although the buffer was not used as loop buffer, one of ordinary skill in the art should be able to recognize Fleck's loop buffer which was used in addition to a cache subsystem (see col.2, lines 49-55) for storing instructions frequently used to minimize the memory

access time (Col. 1, lines 65-67, coil.2, lines 1-2) could have provided a solution to Patel's cache array, and, and in doing so provided a motivation.

With regard to claim 2, Patel also included determining if a portion of address was equal [tag matched] to a tag (e.g. see fig.5 [88], col.8, lines 1-41).

With regard to claim 3, Patel also compared the portion address corresponding to instruction (See the address information in descriptive bits in fig.4) with the tag address (see the tag address from the cache tag array (see col.8, lines 31-68).

Claims 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al. (5,353,426) in view of Fleck et al. (6,085,315) as applied to claim 1 above, and further in view of Uesugi (6,154,814).

Neither Patel nor Fleck disclosed the loading of a tag register after a portion of instruction was in the cache as claimed. As already taught by Patel, an instruction or portion found in the cache was a hit condition by comparing the tag addresses (e.g. see col.9, lines 3-12, see also applicant's specification in page 2, lines 8-15 about the "hit" condition). However, Patel did not specifically teach the loading of a tag register after the hit condition. Nevertheless, Uesugi disclosed a cache system for loading a tag register [16] after a hit occurred (e.g. see eo1.2, lines 33-39, see also co1.2, lines 13-21 for the tag address e.g. see col.6, lines 41-48). It would have been obvious to one of

ordinary skill in the art to use Uesugi in Patel for loading a tag register after a hit as claimed because the use of Uesugi could provide Patel greater flexibilities for adapting specific processing requirements, such as saving an extra copy or updated version of the tag address to minimize the access deadlock of future hits or misses, and it could be readily done by defining a tag register, such as the one taught by Uesugi, into the configuration parameters of Patel (e.g. the bit length, register type etc.) so the tag register of Uesugi could be recognized by Patel, and for the reasons set forth above, provided a motivation.

With regard to claim 7, the value of Uesugi's tag register was also a storage location (see the address stored in the EA register in col.2, lines 21-38).

Claims 9, 10, 18,19, and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jouppi (5,958,040) in view of Bobick et al. (6,535,583).

With regard to claim 9, Jouppi disclosed a cache memory system including at least:

a) determining if a first piece of data is in a buffer (e.g. the comparison of the data address with the tag in the entry of the buffer [310] in col.l0, lines 46, see figs.3, 5);

b) enabling a portion of a memory array [cache] corresponding to the entry of the buffer (e g see the transfer of the corresponding cache line in co1.10, lines 52-54).

Jouppi did not specifically teach his memory array included the loop buffer as claimed.

However, Bobick disclosed a loop buffer [140] included in a memory array [16] (see fig.3, col.10, lines 10-18). It would have been obvious to one of ordinary skill in the art to use Bobick in Jouppi for including the loop buffer in the memory array as claimed because the use of Bobick could provide the processing ability of Jouppi to accept a predetermined set of repeatedly executed instructions at a given request and at a given set of address space, thereby minimizing the access cycle (e.g. without additional control lines) and the hardware overheads of the circuits, although Jouppi's memory array [cache] and the buffer ware separate memories, Bobick , provided the solution by disclosing an integrated structure of the loop buffer with the memory array, one of ordinary skill in the art should be able to recognize the advantage the integrated structure taught by Bobick would be applicable in Jouppi to achieve the enhanced processing speed in the memory system as Jouppi did suggest the desirability of integrating the cache and the buffer in a larger module structure (e.g. see col.3, lines 60-64), and in doing so, provided a motivation.

With regard to claim 10, Jouppi also enabled only the portion comprising the first piece of data (see only the cache line being transferred in co1.10, lines 52-54)

With regard to claim 18, Jouppi also included a tag lookup (see the search in the entries in the tag queue before the full in (col.10, lines 43-67).

With regard to claims 19,21, Jouppi was applicable to a DSP processing because it was CISC and RISC processing. In addition, Bobick was directed to a DSP processing (see fig. I DSP processor).

With regard to claim 20, Jouppi disclosed a cache and a buffer (e.g see fig. 1). Jouppi did not specifically teach his cache and buffer were adapted in a memory array as claimed. However, Bobick disclosed a loop buffer [140] included in a memory array [16] (see fig.3, co1.10, lines 10 18). It would have been obvious to one of ordinary skill in the art to use Bobick in Jouppi for including the memory array adapted to include the loop buffer and the cache as claimed because the use of Bobick could provide the processing ability of Jouppi to accept a predetermined group of repeatedly executed instructions at a given request and at a given set of address space, thereby minimizing the access cycle (e.g. without additional control lines) and the hardware overheads of the circuits, although Jouppi's cache and the buffer ware separate memories, Bobick provided a loop buffer integrated into a memory array [16], and one of ordinary skill in the art should be able to recognize the advantage the integrated structure taught by Bobick would be applicable in Jouppi to achieve the enhanced processing speed in the memory system as Jouppi did suggest the desirability of integrating the cache and the buffer in a larger module structure (e.g. see col.3, lines 60-64), and for the above reasons, provided a suggestion to combine.

With regard to claims, 22, 23, Bobick's memory array [16] also included fixed locations because the loop buffer was physically structured into the RAM [16] (e.g. fig.3). AS for the variable locations set forth in claim 23, variable locations were also applicable in Bobick because Bobick disclosed that his RAM was mapped to respective address space (e.g. see col.6, lines 30-34).

Allowable Subject Matter

Claims 4, 5, 8, and 11-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi Namazi whose telephone number is 571-272-4209. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on 571-272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mehdi Namazi
March 16, 2006

KEVIN VERBRUGGE
PRIMARY EXAMINER